DAYANANDA SAGAR ACADEMY OF TECHNOLOGY AND MANAGEMENT

(Affilated to Visvesvaraya Technological University,Belagavi & Approved by AICTE,New Delhi)
Opp. Art of Living, Udayapura, Kanakapura Road, Bangalore- 560082
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Accredited NBA, NAAC with A+, New Delhi

Faculty Name	**VASUDEVA G**
Academic Designation	**Assistant Professor**
Educational Qualification	**BE, M. Tech,(Ph.D)**
Experience in Years	**10**
Area of Interest	**FinFET technology, DAC design, SAR based ADC design**
Date of Birth	**21/03/1985**
Email ID	**vasudeva-ece@dsatm.edu.in** **devan.vasu921@gmail.com**

Educational Details

- Ph.D. pursuing at RVCE research Centre with thesis submitted in the field of SAR Based ADC design using FinFETs-2013 registered.
- M.Tech in VLSI Design and Embedded systems studied at JSS academy of technical education, Bangalore. Secured First class and passed in the year 2008.
- B.E. in Electronics and Communication Engineering department at Nagarjuna college of Engineering and technology, Bangalore. Secured First class and passed in the year 2006.
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Personal Details

- Date of Birth:21/03/1985
- Hobbies: Traveling, listening to music
- Languages Known: English & Kannada

ProfessionalExperience

1. Worked as Assistant Professor in the department of ECE at Atria Institute of technology, Bangalore from July 2016 to June 2020.
2. Worked as Assistant Professor in the department of ECE at RV College of Engineering, Bangalore from September 2013 to March 2015.
3. Worked as Assistant Professor in the department of ECE at ACS College of Engineering, Bangalore from July 2012 to September 2013.
4. Worked as Lecturer in the department of ECE at Rajiv Gandhi Institute of technology,

Bangalore from August 2009 to July 2012.

Publications

International Journals

1. Vasudeva G, Cyril PrasannaRaj.P "Study of 8 bits Fast Multipliers for low Power applications" ,International Journal of Soft Computing and Research Journal(IJSCE Journal) ,ISSN:2231-2307(ONLINE),March 2015,Impact Factor: 1.275 for the year 2014, Vol 5 ,Issue 1.pp1-7.

2. Vasudeva G " Design of sequential and combinational multipliers by comparing constraints at 130nm technology" at International Journal of Modern Trends in Engineering and Research Journal(IJMTER) Journal(SJIF:1.711) ,Vol2, Issue 8,August 2015, e-ISSN:2349-9745,p-ISSN:2393-8161,pp76-89.

3. Vasudeva G " Design and implementation of Radix-2 Modified Booths Encoder using FPGA and ASIC Methodology" at International Journal of Recent Technology and Engineering Journal (IJRTE) Journal,Impact Factor:1.0 ,ISSN:2277-3878,Vol 4,Issue 3, July 2015, pp43-47.

4. Vasudeva G,Kiran bailey, Kiran K Kalyani "Low power High speed multipliers" at International Journal of Modern Trends in Engineering and Research Journal (IJMTER) Journal,Scientific Journal Impact Factor (SJIF:3.518),Vol 3,Issue 4,April 2016,pp746-750.

5. Vasudeva G, Subodh Kumar Panda, Anoop H K"Implementation of single bit Error detection and Correction using Embedded hamming scheme" at International Journal of Modern Trends in Engineering and Research Journal(IJMTER Journal), Scientific JournalImpactFactor(SJIF:3.518),ISSN(Online):2349-9745,ISSN(Print):2393-8161,Vol 3,Issue 5,May 2016,pp88-94.

6. Vasudeva G, Girish J R, Shankar " Design of High Performance CMOS Comparator using 90nm Technology"at International Journal of Modern Trends in Engineering and ResearchJournal(IJMTERJournal),JournalImpactFactor(SJIF:3.518),ISSN(Online):2349-9745,ISSN(Print):2393-8161Vol 3, Issue 5,May 2016, pp 333-337.

7. Vasudeva G, Venkatesh S N " Design of Modified Booths Encoder With Power Suppression Technique" ,at International Journal of Latest Trends in Engineering and Technology(IJLTET)Journal, DOI: http://dx.doi.org/10.21172/1.81.030,e-ISSN:2278-621X,Vol.8,Issue-1,January-2017,pp 222-229.

8. Vasudeva G "Montgomery Multiplier in Galois Field" at International Journal for Science and Advance Research In Technology (IJSART Journal) ,Impact Factor:6.224, Vol 5 Issue 4,April 2019,ISSN 2395-1092,pp 1306-1309.

9. Vasudeva G "FPGA Implementation of Chinese Remainder Theorem Over Residue Modulo" at International Journal of Research in Engineering, Science and Management (IJRESM) Journal,Volume-3, Issue-2, February-2020 www.ijresm.com | ISSN (Online): 2581-5792 pp395-398.

10. Vasudeva G, Uma B V " 22nm FINFET Based High Gain Wide Band Differential Amplifier" at NAUN Journal, Interntaional Journal of Circuits,Systems and Signal Processing,Volume 15, 2021,DOI: 10.46300/9106.2021.15.7,E-ISSN: 1998-4464,pp 55-62, SCOPUS Indexed Journal and also Indexed in IET In spec and EI Compendex.

11. VasudevaG,Uma B V " Design of OTA based Comparator for High Frequency Applications using 22nm FINFET Technology" at International Journal of Electrical and Computer Engineering (IJECE) Journal. SCOPUS Indexed Journal.SNIP: 1.059; SJR: 0.322; Cite Score: 2.3.

12. VasudevaG,Uma B V "Design and Implementation of High Speed and Low Power 12-bit SAR ADC using 22nm FinFET", at WSEAS transactions on systems and Control, Scopus indexed Journal.

13. Vasudeva G., Uma B. V., "Low Voltage Low Power and High Speed OPAMP Design using High-K FinFET Device," WSEAS Transactions on Circuits and Systems, vol. 20, pp. 80-87, 2021.

National Conferences:

1. Participated and Presented a paper in the National Conference on "Recent Trends In Communication Technology" held at Karnataka State Higher Education Council,Palace Road,Bengaluru-560001 in Association With Centre for Industrial Computers Tumkur university sponsored by Karnataka state Higher Education Council on 13th Jan 2012.Attended from Rajiv Gandhi Institute of Technology,Bangalore.Paper titled: "Design and realization of Low Noise Operational Amplifier with current Driving Bulk using CMOS technology".

2. Participated and Published a Paper entitled "Study of Design and Development of 8-Bit Fast Multiplier for Low Power Applications" in the two days National Conference on "ADVANCED COMMUNICATION TRENDS" ACT 2012 on 23rd& 24th August 2012.

3. Participated and Presented a paper at National Conference on Emerging Trends in VLSI Design and Embedded Systems (ETVDES) Conference on 25th October 2013, attended from R V College of Engineering, Bangalore, Conducted at BMS INTITUTE OF TECHNOLOGY, Yelahanka, Bangalore-64, Titled "Design of Radix-2 Modified Booth's Encoder using FPGA

and ASIC Methodology". Co-Author: Prof. J.R. Girish from SJB INSTITUTE OF TECHNOLOGY, Bangalore.

Academic Activity

1. Worked as a IEEE student chapter coordinator.
2. Worked as department placement coordinator.

Faculty Development Activity/Workshops

1. Attended a 2-Day workshop at REVA Institute of Technology and Management, Kattigenahalli, Yelahanka, Bangalore-64 on "VLSI DESIGN VERIFICATION" on 29th July and 30th July 2010 from Rajiv Gandhi Institute of Technology, Bengaluru.
2. Attended a 3-Day Training Program from 3/1/2012 to 5/1/2012 on "Analog and Digital Design" held at Cadence Design Systems, Bangalore.
3. Participated in the 4-Day VTU-VGST Faculty Development Program from ACS College of Engineering, Bangalore on "VLSI System on Chip and Validation" from 10th July 2013 to 13th July 2013 Organized by R & D Centre and ECE Department, M.S.Engineering College, NavarathnaAgrahara,Sadahalli Post ,off Bangalore International Airport Road,Bangalore-562110.
4. Participated in 5-Day workshop from RV College of Engineering, Bangalore on "Faculty Pedagogical Development Programme" Organized by International Academy for Competency Enhancement, Bangalore from 15/7/2014 to 19/7/2014.
5. Participated in the Workshop on "Geospatial Technology and its Applications" from RV College of Engineering, Bangalore from 4th -6th December 2013 as a part of Institution Academic Networking Programme under TEQIP-II from Sir M Visvesvaraya Geospatial Chair, Indian Institute of Science, Department of Civil Engineering, Information Science and Instrumentation Technology, RashtreeyaVidyalaya College of Engineering(RVCE) and Karnataka State Council for Science & Technology(KSCST).
6. Attended a Faculty Development Programme on "Personality Development" Conducted by Department of Management Studies & Research on 22nd& 23rd July 2015 at Don Bosco Institute of Technology, Kumbalagodu, Mysore road, Bangalore-560074.
7. Attended a Faculty Development Programme on "Physical Design challenges in DSM Node VLSI Systems", Organized by Department of Electronics and Communication Engineering, B.N.M. Institute of Technology, Bengaluru, -560070, during 16th to 21st January 2017.
8. Attended a Faculty Development Programme at Hotel Atria, Bangalore on "Pedagogy training".

9. Attended a Faculty Development Programme on “Latest Trends In Wireless Communiction” Organized by Department of Electronics and Communication Engineering , in association with Jetking Sadashivnagar , held on 24th July 2017 at Atria Institute of Technology,Bengaluru-560024.
10. Attended a Faculty Development Programme on “IOT and Embedded Systems” Organized by Department of Electronics and Communication Engineering , Atria Institute of Technology ,Anandnagar,Bengaluru-560024 , Karnataka during 22nd to 27th January 2018.
11. Attended a one week workshop on “RTOS and Machine Learning in the Edge Devices” held on 14th Jan 2019 to 19th Jan 2019 organized by the Department of Electronics and Communication Engineering ,Atria Institute of Technology, Bangalore-24.
12. Attended a 2-Day workshop on “VLSI design flow using Xilinx Vivado” held from 28th to 29th January 2019,organized by the Department of Electronics and Communication Engineering, Atria Institute of Technology,Bengaluru-24.
13. Attended a online Workshop Conducted by Department of Electronics and Communication Engineering, TEQIP(Phase-III) Sponsored on “Recent Trends in VLSI Devices/Circuits and Applications” held at Malaviya National Institute of Technology,Jaipur, from 1st October to 5th October 2020.
14. Attended a online workshop Conducted by Department of Electronics and Communication Engineering ,TEQIP(Phase-III) Sponsored Five Days from 26th November 2020 to 30th November 2020 on “Emerging CMOS Technologies and Beyond: Trends and Challenges” held at Malaviya National Institute of Technology,Jaipur.

Contact Details

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